



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,597	09/16/2003	Stephen W. Spriggs	TI-35269	3951
23494	7590	02/23/2006	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			HEIN, GREGORY P	
			ART UNIT	PAPER NUMBER
			2188	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,597	SPRIGGS ET AL.	
	Examiner Gregory P. Hein	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 16 September 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1 - 21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1 - 3, 5 - 6, and 10 - 13 is/are rejected.
- 7) Claim(s) 4, 7 - 9, and 14 - 21 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 16 September 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>9/16/2003</u> .	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 9/16/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

2. Claims 13 - 14 and 17 are objected to because of the following informalities:

Line 4 and line 17 of claims 14 and 17, respectively, read "internal cock signal." Examiner believes this should read "internal clock signal."

Lines 4 – 5 of claim 14 read "whether the memory device sin a burst mode of operation." Examiner believes this should read whether the memory device is in a burst mode of operation."

Line 3 of claim 13 has a repetitive use of value.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 6 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Art Unit: 2188

5. As written "...a function of..." on line 3 of claim 13 is indefinite language.

The causal relationship could reasonably be interpreted as between the time period and the listed factors or between the value and the listed factors.

6. Claim 13 states "respectively" on line 4. The language used here is indefinite since no intended corresponding list can be ascertained from the claim.

7. The term "substantially" in claims 6 and 12 is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1 – 3 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,239,639 (Fischer et al.).

10. As per claim 1, Fischer teaches:

A memory array (Fischer Col. 5 lines 1 – 11);

A memory input circuit operable to receive an input clock signal and generate a memory operation initiation signal in response thereto (Fischer Col. 7

Art Unit: 2188

lines 25 – 31 “...a cycle start signal is sent to state tracker ... in response to the cycle start signal, the state tracker activates the start strobe signal...”); and

A memory control circuit operable to receive the memory operation initiation signal and generate one or more control signals to initiate a memory operation in response thereto, the memory control circuit further operable to identify completion of the memory operation and generate a cycle ready strobe signal in response thereto (Fischer Col. 7 lines 29 – 31 and Fischer Col. 7 lines 5 – 7 The memory controller determines the time necessary to complete the memory operation and communicates this to the tracker.).

Wherein the memory input circuit receives the cycle ready strobe signal as an input and generates a next memory operation initiation signal in response thereto for initiation of a next memory operation (Fischer Col. 7 lines 59 – 64 The delay is communicated and after the delay period the memory operation is complete.)

As per claim 2, Fischer teaches:

A bit line pre-charge circuit operable to pre-charge one or more bit lines of the memory array to a predetermined potential after a memory operation is completed in response to enabling a bit line pre-charge signal as one of the one or more control signals of the memory control circuit (Fischer Col. 5 lines 18 – 22.)

As per claim 3, Fischer teaches:

The memory control circuit further comprises a cycle ready circuit operable to generate the cycle ready strobe signal in response to the enabling of

the bit line pre-charge signal (Fischer Col. 5 lines 18 – 22. The memory controller contains logic to assert the RAS and CAS with appropriate delays.)

As per claim 5, Fischer teaches:

The cycle ready circuit is further operable to generate the cycle ready strobe signal a predetermined period of time after the enabling of the bit line pre-charge signal (Fischer Col. 5 lines 18 – 22.)

As per claim 6, Fischer teaches:

The predetermined period of time is sufficient to ensure that the true and complement bit lines associated with a selected memory cell within the memory array are substantially equalized and have reached a predetermined voltage level (Fischer Col. 7 lines 7 - 15

As per claim 10, Fischer teaches:

A memory array (Fischer Col. 5 lines 1 – 11); and
A memory control circuit operable to initiate a first memory operation based on an external system clock (Fischer Col. 7 lines 25 – 31), and initiate a second memory operation based on an indication that the first memory operation is complete (Fischer Col. 7 lines 59 – 64 and Col. 7 lines 7 – 15.)

As per claim 11, Fischer teaches:

The memory control circuit is operable to detect completion of the first memory operation and generate a cycle ready signal for initiation of the second memory operation (Fischer Col. 7 lines 3 – 15.)

As per claim 12, Fischer teaches:

The memory control circuit is operable to generate the cycle ready signal a predetermined period of time after a bit line pre-charge signal is enabled, wherein the predetermined period of time is sufficient to ensure that true and complement bit lines associated with a selected memory cell substantially equalize and reach a predetermined value (Fischer Col. 5 lines 18 – 22 The memory controller contains logic to assert the RAS and CAS with appropriate delays.)

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,239,639 (Fischer et al.) and further in view of U.S. Patent 6,434,082 (Hovis et al.)

13. As per claim 13:

Fischer does not teach that the delay in the pre-charge is explicitly due to temperature, supply voltage or process variation factors.

Hovis teaches that variations in temperature and supply voltage can introduce unwanted delays into the system. It would have been obvious to one

of ordinary skill in the art at the time of the invention that temperature and supply voltages can affect delay times (Hovis Col. 4 lines 8 – 11)

Allowable Subject Matter

14. Claims 4, 7 – 9, and 14 - 21 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory P. Hein whose telephone number is 571-272-4180. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2188

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/14/2006
Gregory Hein

Mano Padmanabhan
Mano Padmanabhan
SPO/106

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER